

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-32. (Canceled)

Please add the claims 33-42 as follows:

33. (New) A liquid crystal display including an array of thin film transistors (TFTs), comprising:

a substantially transparent first substrate;

an array of TFT gate electrodes and gate address lines;

a semiconductor layer on the first substrate over the gate electrodes;

drain and source electrodes on the substrate over the semiconductor layer;

drain address lines addressing the drain electrodes;

a substantially continuous organic insulating layer on the substrate over the address lines and the drain and source electrodes, the substantially continuous organic insulating layer having a thickness of at least about 1.5 μm ; and

an array of substantially transparent pixel electrodes on the substrate over the insulating layer so that the patterned pixel electrodes overlap the gate and drain lines in order to increase a pixel aperture ratio of the display,

wherein a parasitic capacitance corresponding to an overlap of each of the pixel electrodes with one of the gate and drain lines is no greater than 0.01pF.

34. (New) The liquid crystal display of claim 33, wherein a pixel pitch of the display is about 150 μm .

35. (New) The liquid crystal display of claim 33, wherein the organic insulating layer includes Benzocyclobutene (BCB).

36. (New) The liquid crystal display of claim 33, wherein the organic insulating layer has a dielectric constant of less than about 3.0.

37. (New) An array of thin film transistors (TFTs), comprising:

- a substrate;
- an array of TFTs on the substrate, each TFT including a gate, source and drain;
- a plurality of address lines on the substrate for addressing the array of TFTs;
- an insulating layer including Benzocyclobutene (BCB) over the array of TFTs and over the address lines; and
- an array of substantially transparent pixel electrodes on the substrate over the insulating layer so that the pixel electrodes overlap the address lines in order to increase a pixel aperture ratio of the display,

wherein a parasitic capacitance corresponding to an overlap of one of the pixel electrodes with one of the address lines is no greater than 0.01pF.

38. (New) The array of claim 37, wherein a pixel pitch of the display is about 150 μm .

39. (New) An array of thin film transistors (TFTs), comprising:
- a substrate;
 - an array of TFT gate electrodes and gate address lines on the substrate;
 - a semiconductor layer over the gate electrodes on the substrate;
 - a plurality of drain address lines on the substrate;
 - an array of TFT drain and source electrodes on the substrate over the semiconductor layer so as to form the array of TFTs;
 - an organic insulating layer having a dielectric constant of less than about 3.0 on the substrate over the source and drain electrodes; and
 - an array of pixel electrodes over the insulating layer and overlapping the gate and drain address lines,
- wherein a parasitic capacitance corresponding to an overlap of each of the pixel electrodes with one of the gate and drain address lines is no greater than 0.01pF.
40. (New) The array of claim 39, wherein the organic insulating layer is substantially transparent.
41. (New) The array of claim 39, wherein the organic insulating layer is at least about 1.5 μm thick.
42. (New) The array of claim 41, wherein the organic insulating layer is at least about 1.5 μm thick in an overlap area of the pixel electrode and one of the gate and drain address lines.